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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/556,647
Filing Date: November 10, 2005
Appellant(s): ROBBE ET AL.

J. William Frank
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/21/2009 appealing from the Office action mailed 8/7/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6611161 Kumar 8-2003

Nilson and Riedel "Electric Circuits" , fifth edition, (1996 Addison-Wesley Publishing Company, Inc.), figure 6.17 pp. 227 [ISBN 0-201-55707-X]

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan (US 6693494) in view of (Nilson and Riedel, Electric Circuits fifth edition figure 6.17 pg 227)

3. With respect to claim 1, figures 6, 4 and 3 of Fan (US 6693494) discloses a voltage shift control circuit intended to be placed in parallel with at least one voltage shift capacitor (C1) coupling the phase comparator (21) and the voltage controlled oscillator (23) of a phase locked loop, and comprising: an input (input to the charge pump A), intended to be coupled with the output of the phase comparator; an output (output of the loop filter 22), intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (FIG 6), designed to charge the voltage shift capacitor (C3) according to a control signal (NORMAL MODE, SPEEDUP MODE OR PRECHARGE MODE); controlled pre-charging means (62, 63, 64, 65, Sb and Sc),

designed to accelerate (via SPEEDUP MODE) the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means (40 of figure 4), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor but fails to disclose at least one series voltage shift capacitor. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 7, the above combination discloses the circuit according to Claim 1, further comprising means (Sc) for deactivating the controlled pre-charging means before the controlled polarization means.

With respect to claim 10, the above combination discloses the circuit according to claim 1, designed in CMOS technology (Note this claim is deemed obvious expedient to one skilled in the art to design the circuit using CMOS technology).

With respect to claim 11, the combination above discloses the Phase locked loop comprising a phase or frequency comparator (21), a loop filter (22), a voltage controlled oscillator (23), a voltage shift capacitor (C3) connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor (C3) and comprising : an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator (23); controlled charging

means (60, 61), designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means(62, 63, 64, 65, Sb and Sc), designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means (40), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor but fails to disclose a series voltage shift capacitor. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 12, the combination above discloses the Radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), phase locked loop generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a Voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (60, 61), designed to charge the voltage shift capacitor according to a control signal; controlled pre-charring means (62, 63, 64, 65, Sb and Sc), designed to accelerate the charging of the

voltage shift capacitor by the controlled charging means; and controlled polarization means (40), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

With respect to claim 13, the combination above discloses the Mobile terminal of a radio-communications system with a radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter and the Mobile terminal is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), having a phase locked loop for generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charging means, designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

With respect to claim 14, the combination above discloses the Base station of a radio-communications system with a radio-frequency transmitter (Note: the recitation of the Radio frequency transmitter and the Base station is deemed intended use because the circuit of claim 1 can be put into a variety of circuits), having a phase locked loop for

generating a radio-frequency signal to be transmitted, said phase locked loop comprising a phase or frequency comparator, a loop filter, a voltage controlled oscillator, a voltage shift capacitor connecting the phase comparator and the voltage controlled oscillator, and a voltage shift control circuit according to Claim 1 placed in parallel with the voltage shift capacitor and comprising: an input, intended to be coupled with the output of the phase comparator; an output, intended to be coupled with the input of the voltage controlled oscillator; controlled charring means, designed to charge the voltage shift capacitor according to a control signal; controlled pre-charging means, designed to accelerate the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization means, designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor.

4. Claims 2-5, 8 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Fan (US 6693494) in view of Kumar et al. (US 6611161) in further view of of (Nilson and Riedel, Electric Circuits fifth edition figure 6.17 pg 227)

With respect to claim 2, figures 6, 4 and 3 of Fan (US 6693494) discloses a voltage shift control circuit intended to be placed in parallel with at least one voltage shift capacitor (C1) coupling the phase comparator (21) and the voltage controlled oscillator (23) of a phase locked loop, and comprising: an input (input to the charge pump A), intended to be coupled with the output of the phase comparator; an output (out of 22), intended to be coupled with the input of the voltage controlled oscillator; controlled charging means (FIG 6), designed to charge the voltage shift capacitor (C3)

according to a control signal (NORMAL MODE, SPEEDUP MODE OR PRECHARGE MODE); controlled pre-charging means (62, 63, 64, 65, Sb and Sc), designed to accelerate (via SPEEDUP MODE) the charging of the voltage shift capacitor by the controlled charging means; and controlled polarization (division into two opposites) means (40 of figure 4), designed to ensure the polarization of the input during the pre-charging of the voltage shift capacitor but fails to disclose wherein the controlled charging means comprise a first operational amplifier connected as a voltage follower between the input and the output, a resistor (R3) placed in the feedback loop of the operational amplifier, and a controlled current source (60) supplying a current (at node output from 60) of specified value through said resistor and fails to disclose a series voltage shift capacitor. Figure 4 of Kumar teaches the use of a unity gain amplifier (240) at the output of the charge pump to suppress charge sharing from parasitic capacitances. It would have been obvious at the time the invention was made to use the unity gain amplifier of Kumar in the circuit of Fan for the purpose of suppressing charge sharing from parasitic capacitances. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a larger equivalent capacitor for the well known purpose of optimizing the value of the capacitance.

With respect to claim 3, the combination above discloses the circuit according to Claim 2, wherein the operational amplifier of the charging means comprise a push-pull output stage (60 and 61)-and wherein the charging means further comprise a resistor

(R3) of high value connected in series between the output of the operational amplifier and the output of the circuit.

With respect to claim 4, the combination above discloses the circuit according to Claim 3, wherein the controlled pre-charging means comprise a push-pull stage (64 65) which, in the activation of the pre-charging means configuration, is arranged as a mirror with respect to the push-pull output stage of the operational amplifier of the charging means, in such a way as to short-circuit the high value resistor.

With respect to claim 5, figure discloses the circuit according to Claim 4, wherein the push-pull stage (64 and 65) of the pre-charging means (62, 63, 64, 65, Sb and Sc) is designed to deliver a current higher than the current delivered by the push-pull output stage of the operational amplifier of the charging means.

With respect to claim 8, the combination above discloses circuit according to Claim 2 further comprising an additional controlled push-pull stage (62 and 63) whose output is intended to be connected to the centre point of an RC network of a loop filter (22) of the PLL and which, in the activation configuration, is connected as a mirror with respect to the push-pull stage (64 and 65) of the controlled pre-charging (62, 63, 64, 65, Sb and Sc) means and with respect to the push-pull output stage of the operational amplifier of the charging means.

With respect to claim 9, the combination above discloses circuit according to Claim 8, wherein the additional controlled push-pull stage (62 and 63) is integrated with the operational amplifier of the charging means.

(10) Response to Argument

A. With respect to Appellant's argument that Claims 1, 7 and 10-14 are not obvious over Fan in view of Riedel because Fan and Reidel do not disclose or suggest at least one series voltage shift capacitor coupling a phase comparator and a voltage controlled oscillator of a phase locked loop, the Examiner disagrees. The Appellant goes on to argue the limitation of "at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop" is not disclosed. The Examiner argues that the phase comparator is element 21 of figure 3 and 4 of Fan. The voltage controlled oscillator is element 23 of Fan. The voltage shift capacitor is element C1 of Fan.

The Examiner agrees that element C1 of Fan by itself is not a series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase lock loop because it is not coupled in series. The teaching of Nilson and Riedel teaches that a capacitor can be made up of several capacitors in series. In view of this teaching replacing the capacitor C1 of Fan with a number of capacitors in series would make each of the capacitors of the series a series capacitor. Each one of the multiple capacitors is coupled to the phase comparator and the voltage controlled oscillator.

With respect to Appellant's argument that the quoted language from claim 1 clearly states that the capacitor is coupled in series between the phase comparator and the voltage controlled oscillator of a phase locked loop, the Examiner disagrees. The claim language does not state that the capacitor is "coupled in series between" but rather the "series voltage shift capacitor" is "coupling the phase comparator and the

voltage controlled oscillator", which conveys two entirely different meanings. The first interpretation meaning that the phase comparator is in series with the capacitor which is in series with the oscillator. The second interpretation meaning that a series capacitor is coupled to a phase comparator and a voltage controlled oscillator. One skilled in the art would interpret (as the Examiner has) the claim language to invoke the second meaning.

With respect to Appellants argument that, "the examiner briefly states C1 and C3 are series capacitors coupling the phase comparator and the VCO as stated in the rejection." However, in Figure 6 of Fan, capacitors C1 and C3 are clearly connected to ground and would be considered as "parallel capacitors" by one of ordinary skill in the art. Therefore, the examiner's assertion that the capacitors (C1 and C3) disclose the series capacitors recited by claims 1, 7 and 10-14 is clearly an error." the Examiner disagrees. In view of the Nielson Riedel reference C1 and C3 each would be made up of numerous capacitors and each of the individual capacitors would be a series capacitor. The fact that the capacitors are connected to ground reinforces the face that the voltage shift control circuit is placed in parallel with the at least one series voltage shift capacitor. The parallel nature of the voltage shift control circuit and the voltage shift capacitor being demonstrated in the fact that both of the voltage shift capacitor and the voltage shift control circuit are connected to each other and to ground.

With respect to Appellant's argument none of the other applied references supplies these deficiencies of Fan and Riedel, the Examiner points out in view of the

above arguments the combination of Fan and Riedel as interpreted meet the claim limitations.

B. With respect to Appellant's argument that "Claims 1, 7 and 10-14 are not obvious over Fan in view of Riedel because Fan and Riedel do not disclose or suggest controlled polarization means designed to ensure the polarization of an input during the pre-charging of the voltage shift capacitor.", the Examiner disagrees. As discussed in the rejection above the Examiner maintains that the polarizing means is element 40 of figure 4 of Fan. The input in question as stated by the Appellant is the input to charge pump A. The output of charge pump B is connected at the same node as the input of charge pump A and the switch SB being on or off controls the charge pump B. Whether the switch is on or off is controlled by the 1-bit quantizer. "1-bit quantizer 40 then also controls switch Sb to control synthesizer 20 from speed up mode to normal mode" (column 5 lines 11-13) The switch Sb has two states or quantum on and off. According to Webster's dictionary 10th edition the standard definition of polarization is a division into two opposites. Therefore, the 1 bit quantizer has the function of polarizing the switch Sb into two opposites (on or off) which is the input of the chargepump A as seen in figure 6. During pre-charge mode, which is when the switch Sc is closed, the speedup mode is polarized to off (i.e SB is open). Therefore the controlled polarization means (40) ensures the polarization (on or off) of the input (input to the Charge pump A) during the pre-charging (when the Sc switch is closed) of the voltage shift capacitor. As such it is believed by the Examiner, that Fan in view of Nielson and Riedel reads on the claim limitation.

C. With respect to Apellant's argument that claims 2-5, 8 and 9 are allowable for at least the same reasons presented in sections 7(A) and 7(B) herein above because such claims are dependent upon independent claim 1 and stand or fall with independent claim 1, the Examiner disagrees. Although he claims 2-5, 8 and 9 do stand and fall with independent claim 1, the Examiner for reasons above believe the prior art cited read on the above claim limitations and therefore the cited claims remain rejected.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Khareem E Almo/

Examiner, Art Unit 2816

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